Amendments to the Specification:

Paragraph beginning on page 1, line 9

Currently, ~~the demand~~ worldwide demand for wireless services is growing at ~~a fast~~ an ever quickening pace. This demand is not only for an increased number of users but also for extended wireless access capabilities. These capabilities include for example, Internet access, video conferencing and multimedia applications.

Paragraph beginning on page 1, line 13

Code Division Multiple Access (CDMA) and Wideband-CDMA (W-CDMA) are spread spectrum based broadband communications technologies that are becoming increasingly popular in mobile wireless communication systems and, in particular, for 3G mobile systems currently under development. In a CDMA system, all users simultaneously occupy the same frequency[[ ]]. In contrast, ~~different~~ users in Frequency Division Multiple Access (FDMA) systems ~~receive~~ communicate over separate frequencies. Users in Time Division Multiple Access (TDMA) systems receive and transmit data during separate predefined time slots. CDMA systems, however, discriminate between users by ~~using~~ assigning a different ~~codes~~ code for each user. In the downlink, CDMA base stations simultaneously transmit signals to multiple subscriber mobile stations over a single frequency band whereby each signal is generated using a different code associated with each user. Several advantages of CDMA systems over other multiple access systems such as FDMA and TDMA systems include greatly increased spectral efficiently and the ability to reduce the affects of signal fading by making use of known path diversity techniques.

Paragraph beginning on page 5, line 8

In one embodiment, the correlator is adapted to correlate an input Rx signal sampled at an ~~over sampling~~ over-sampling rate with a single code wherein multiple correlations are performed for each ~~over sampling~~ over-sampling phase within the nominal sample period. Separate integration result registers are employed to store the individual correlation sums.

Paragraph beginning on page 9, line 19

Fig. 8 is a block diagram illustrating the collapsed finger bank ~~construction~~ constructed in accordance with the present invention in more detail.

Paragraph beginning on page 11, line 9

It is noted that the present invention is not limited to use with any particular code. Throughout this document the invention is described in reference to W-CDMA codes but it is not

limited [[to]] for use with only these codes. Depending on the particular application and implementation, the invention is applicable for use with a multitude of types and varieties of codes including different phases of the same code. Examples include but are not limited to PN codes such as used in IS-95, Gold sequences and complex Gold sequences used in W-CDMA and cdma2000, channelization codes, OVSF codes, Walsh or Hadamard codes, scrambling codes, etc.

Paragraph beginning on page 11, line 17

Throughout this document the term nominal sampling rate is defined as the basic chip rate of a spread spectrum signal. The sample rate is defined as the actual input sample rate which typically comprises an ~~over-sampling~~ over-sampling rate or fractional space chip rate. For example a number of samples N may be generated within each chip period. The N fractional spaced samples are input at the sample rate which is N times the nominal sample rate or basic chip rate. The effective sample rate is the sample rate gated against a SAMPLE ENABLE signal whereby E < N samples per chip period are to be correlated. The effective sample rate is then E times the nominal sample rate.

Paragraph beginning on page 11, line 32

A block diagram of a first embodiment of the correlator of the present invention incorporating a single sample register and a single code register is shown in Figure 2. In this embodiment, the correlator, generally referenced 30, is adapted to correlate an input receive signal sampled at an ~~over-sampling~~ over-sampling rate with a single code wherein multiple correlations are performed for each ~~over-sampling~~ over-sampling phase within the nominal sample period. Separate integration result registers are employed to store the individual correlation sums.

Paragraph beginning on page 12, line 5

The Rx input 32 comprises received signal samples provided by a receiver front end. The input samples are clocked into a sample register 34 via a SAMPLE CLOCK. A SAMPLE ENABLE signal determines the clock cycles in which a new input sample is clocked into the sample register. The sample register receives data at the ~~over-sampling~~ over-sampling clock rate R which is R times the nominal sample rate. The SAMPLE ENABLE signal determines the number of samples E during the nominal sample time (i.e. basic chip time) actually clocked in resulting in an effective sampling rate of E times the nominal sample rate.

Paragraph beginning on page 12, line 21

The integration results shift register comprises an M-stage shift register wherein each register 56 is adapted to store the intermediate correlation sums. The number of registers M required in this case is equal to the effective over sampling ratio $E \leq R$. The shift register is clocked by an

integration clock (INT CLOCK) enabled by an INT ENABLE signal, which together generate the same rate as the effective sampling rate. The output 59 of the last stage of the shift register is fed back to the adder at the proper time to accumulate the next correlation product. Note that in the case where all the ~~over-samples~~ over-samples in a chip period are to be correlated, the SAMPLE ENABLE signal is not required. The number of result shift registers $M = R$ and the INT CLOCK rate is R times the nominal sample rate.

Paragraph beginning on page 12, line 30

The integration results are appropriately ordered in addition to the appropriate clocking of the sample, code and integration results shift register such that the integration result currently being fed back to the adder corresponds to the multiplication result currently being input to the adder. Thus, each sample is sequentially multiplied by the code and a separate correlation sum is calculated for each ~~over-sampling~~ over-sampling input sample. As correlation sums are accumulated, they are shifted back into the first stage of the integration results shift register.

Paragraph beginning on page 13, line 3

The integration process is halted at the end of the symbol by clearing the particular integration register by applying a zero value at the input to the adder rather than the contents of the register. Thus, the multiplication products of each of the first input samples of the subsequent symbol [[to]] will be stored in the results shift register without any remnants from the previous correlation cycle. A multiplexer 44 is used to select between either the output of the last stage of the results shift register or the zero value in accordance with a RESULT ENABLE signal. The output of the multiplexer 57 makes up the second input to the adder.

Paragraph beginning on page 13, line 23

A suitable application of this embodiment is as the correlator for a single rake finger where the samples are received at an effective over sampling rate $E \leq R$ times the nominal SAMPLE CLOCK rate. In this case, the SAMPLE ENABLE signal is active in accordance with the number of phases to be correlated and only a single code is used. The code register operates at the slower nominal sample clock rate. For each code loaded, E correlations are performed, each with a different ~~over-sampling~~ over-sampling phase. The E results per chip period are stored in the E-stage integration results shift register during the correlation process which is clocked at the clock rate equal to the effective sampling rate. When integration is complete, the correlations results in the results shift register are sequentially clocked out to the results register where they are input to subsequent processing stages.

Paragraph beginning on page 14, line 2

A block diagram of a second embodiment of the correlator of the present invention incorporating a single sample register and a circular code shift register is shown in Figure 3. This embodiment is capable of performing multiple correlations with an ~~over-sampling~~ over-sampling receive signal with multiple codes. It is similar in construction and operation to the correlator of Figure 2 described infra. The codes are stored within a circular shift register that is clocked at a sufficiently high rate such that each input sample is multiplied with all codes. A corresponding number of integration result registers are used to accumulate and store a plurality of correlation sums.

Paragraph beginning on page 14, line 10

The Rx input samples 62 are clocked into a sample register 64 via a SAMPLE CLOCK against a SAMPLE ENABLE signal. The sample register receives data at the ~~over-sampling~~ over-sampling clock rate R which is R times the nominal sample rate. The SAMPLE ENABLE signal determines the number of samples E during the nominal sample time (i.e. basic chip time). ~~actually~~ Actually, the samples are clocked in at the resulting effective sampling rate of E times the nominal sample rate.

Paragraph beginning on page 14, line 16

A number N of codes, provided by code generator 90, are parallel loaded into a circular code shift register 78 in accordance with a code shift register load signal. A new set of N codes is loaded every nominal sample period. The code shift register is clocked at a rate N times the effective sampling clock rate against a CODE/INT ENABLE signal, thus permitting the correlation of fewer then N codes per chip cycle. Assuming all N codes are used and R ~~over-sampling~~ over-samples per chip [[is]] are used, the CODE CLOCK rate is $E \times N \times (\text{nominal clock rate})$. In this case, for every input sample, the contents of the code shift register are circularly shifted one complete revolution, i.e. the code 0 value is circularly shifted until it returns to its starting location. The number of actual correlations performed per chip period ~~maybe~~ may be less than R depending on the effective rate as determined by R and the SAMPLE ENABLE signal.

Paragraph beginning on page 14, line 32

The integration results shift register comprises an M-stage shift register wherein each register 86 is adapted to store the intermediate correlation sums. The number of registers M required in this case is equal to $E \times N$, i.e. the effective ~~over-sampling~~ over-sampling ratio times the number of codes. The results shift register is clocked by an integration clock (INT CLOCK) against the

CODE/INT ENABLE signal. In this case, the CODE CLOCK and INT CLOCK are the same rate, i.e. $E \times N \times$ (nominal clock rate). In the case of $E < R$, one or more INT clock cycles are disabled each chip cycle. The output 94 of the last stage of the shift register is fed back to the adder at the proper time to accumulate the correlation product corresponding to that sample and code being multiplied.

Paragraph beginning on page 16, line 11

A suitable application for this embodiment is its use in channel estimation wherein the sample register is enabled in one or more of the ~~over-sampling~~ over-sampling phases whereby each sample is to be correlated with N codes. The N codes are parallel loaded into the circular code shift register. Using the SAMPLE ENABLE, the rate samples are loaded into the sample register is limited to the enable rate E. Both the code shift register and integration result shift register are clocked at a rate $E \times N \times$ (nominal clock rate). For each of the N codes loaded, E correlations are performed, each with a different phase input sample. The correlation result sums are stored in the result shift register whose length is $M = N \times E$. When the integration period for a code(s) is complete, the result(s) is sequentially clocked out to the results register.

Paragraph beginning on page 16, line 30

A block diagram illustrating a circular sample shift register to be used in place of the single sample register in the correlator of the present invention is shown in Figure 4. The circular sample shift register 100 comprises a P-stage shift register wherein each stage 104 is adapted to hold an individual input sample. The P inputs 102, labeled Rx Input_0 through Rx Input_{P-1} are parallel loaded into the sample shift register in accordance with the sample shift register load signal. The output 106 of the last stage of the sample shift register is fed back to its input stage and to the multiplier input. The contents are circularly shifted at the sample clock rate which is P times the nominal sample clock rate or the ~~over-sampling~~ over-sampling clock rate in the case ~~over-sampling~~ over-sampling is employed. The shift register is loaded at the nominal sample rate or the ~~over-sampling~~ over-sampling rate if ~~over-sampling~~ over-sampling is employed.

Paragraph beginning on page 17, line 7

In operation, for each set of P input samples, the sample shift register is circularly shifted one whole revolution whereby each input sample is multiplied with each of N code values. In this case, the length M of the integration results shift register is increased to $P \times N$ or $R \times P \times N$ in the case of an ~~over-sampled~~ over-sampled input.

Paragraph beginning on page 17, line 11

When the sample shift register is incorporated in the correlator, the shift clock rate for the circular code shift register and the integration results shift register must be increased by P times to compensate for the larger number of input samples that must be correlated within the same sample period. The shift clock rate becomes $P \times N \times$ (nominal clock rate) or $R \times P \times N \times$ (nominal clock rate) in the case of ~~over-sampled~~ over-sampled input.

Paragraph beginning on page 17, line 16

Reduced Complexity Correlator With ~~Over-Sampled~~ Over-Sampled Input
with Multiple Codes and Variable Length Results Shift Register

Paragraph beginning on page 18, line 31

The timing and control unit generates the RESULT ENABLE signal (trace 164) to the results register every four sample clock cycles for $code_0$ and every eight sample clock cycles for $code_1$. The contents of the result register is shown in trace 166. At the sample 4 time, the correlation sum Σ_0 is input to the results register while a zero is simultaneously applied to the adder to clear the correlation sum. Thus, the correlation sum Σ_0 is not added to the multiplication product for sample 4. Similarly, at sample 8, correlation sum Σ_0 is output. At the next sample time, i.e. sample 9, the correlation sum Σ_1 is output to the result register in accordance with the spreading factor SF = 8 for $code_1$.

Paragraph beginning on page 19, line 7

The reduced complexity correlator of the present invention may be incorporated [[in]] within a communications device such as a W-CDMA mobile receiver, W-CDMA base station receiver, etc. A block diagram illustrating an example W-CDMA rake receiver incorporating ~~a collapsed~~ the reduced complexity correlator of the present invention is shown in Figure 7. A W-CDMA receiver, generally referenced 170, for use in a W-CDMA communications system is shown. The receive 170 comprises an antenna element 172, an RF front end circuit 176, an A/D converter 180 and a rake receiver unit 184. The rake receiver comprises an Rx matched filter 186, a collapsed finger bank 190 constructed using the reduced complexity correlator of the present invention, a path selection unit or searcher 192, a maximum ratio combiner (MRC) unit 194, a channel estimation unit 200 and a channel CODEC or forward error correction (FEC) unit 208. It is noted that although the W-CDMA receiver example presented herein is directed towards the ~~receive~~ receiver in the mobile unit, the principles of the present invention may be applied to other applications as well. The invention

can be applied, for example, to the rake receiver in a W-CDMA base station receiver or to any other application that requires a plurality of correlations to be performed.

Paragraph beginning on page 20, line 9

The rake receiver combats these signal impairments by the use of several techniques including channel estimation and tracking, maximum ratio combining to take advantage of multipath, multi-user detection schemes (e.g., interference cancellation or decorrelating receivers), fast power control based on signal-to-interference ratio (SIR) estimation and antenna diversity to provide another form of diversity (i.e. space-diversity) in addition to frequency diversity.

Paragraph beginning on page 21, line 5

The correlators function to multiply the samples by the spreading codes and to accumulate the results using integrators. The correlator function for all the fingers are performed using the reduced complexity correlator of the present invention. Correlations for the early, on-time and late samples are obtained by adjusting the code to generate early, on-time and late code phases. This is equivalent to using the same code [[on]] and using early, on-time and late receive samples. The correlator embodiment of Figure 3 may be used whereby the N codes comprise the various phases of the code sequence the receive signal is to be correlated against.

Paragraph beginning on page 22, line 4

A block diagram illustrating the collapsed finger bank ~~construction~~ constructed in accordance with the present invention in more detail is shown in Figure 8. As described supra, the finger bank in the rake receiver is implemented using the reduced complexity correlator of the present invention. This allows the plurality of finger banks to be 'collapsed' into a single unit.

Paragraph beginning on page 22, line 9

The collapsed finger bank comprises a code ~~generate~~ generator 222 and reduced complexity correlator (RCC) 224 such as that described in connection with Figure 3. In operation, the Rx input samples 188 are input to the RCC 224 while the N codes 226 ($code_0$ through $code_{N-1}$) are provided by the code generator 222. The code generator is adapted to generate all the codes required by the processing to be performed by each 'finger' in de-spreading the multipath assigned to it. The various codes are generated in accordance with the path selection signals 204 provided by the searcher. In addition, N spreading factors (SF_0 through SF_{N-1}) associated with each of the N codes are input to the RCC by the code generator or alternatively by the searcher. As described supra, the spreading factor information is used by the RCC to determine the integration length of each

correlation. Correlation results associated with both the data traffic 196 and the pilot channels 198 are output to the MRC and channel estimation, respectively.